

Teaching Computer Architecture with a Perl based Emulator

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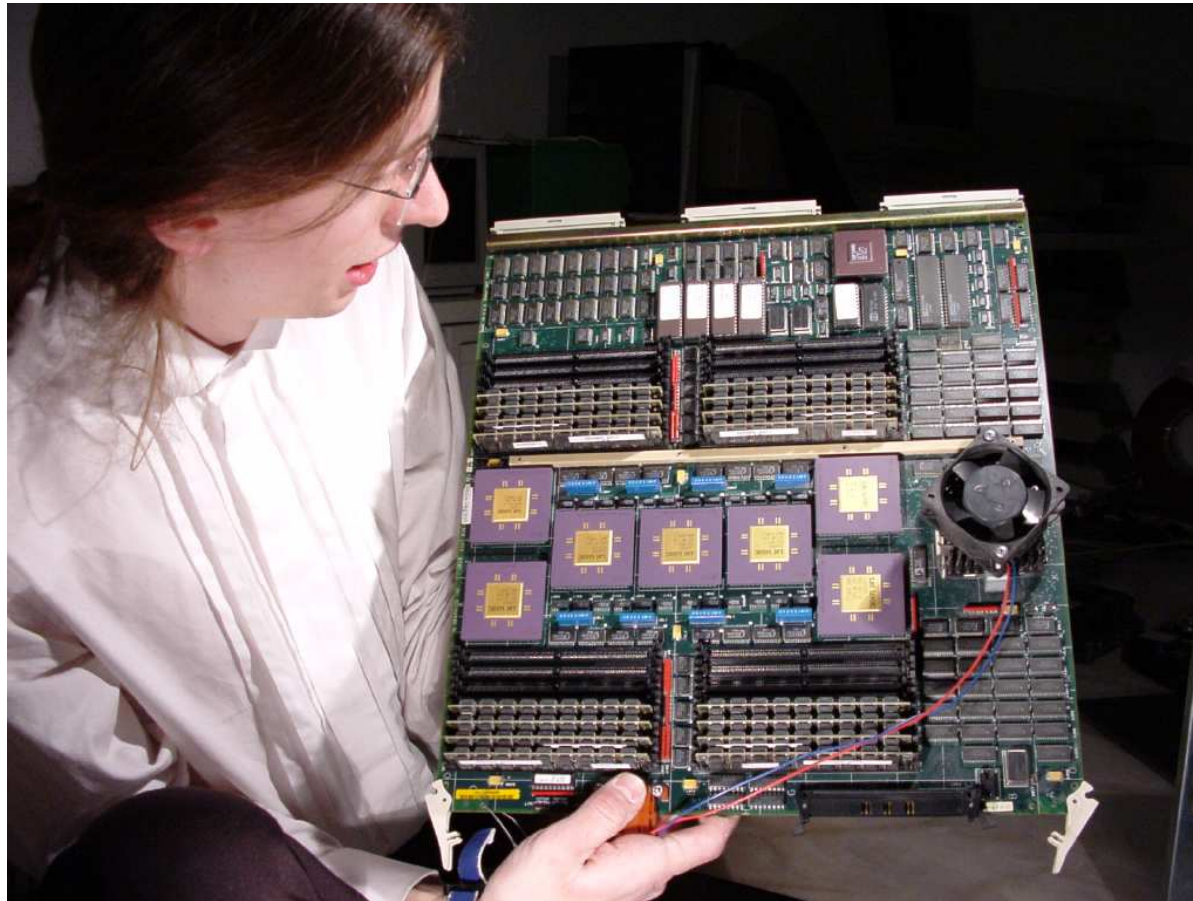
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Why teaching computer architecture?

- ☹ Because I have to in my job as a lecturer. :-)
- ☹ Because people – especially students of computer science – should know about the innards of a digital computer (not just from the standpoint of a high level language programmer).
- ☹ Because people should learn about the concept of beauty in computer architecture – not just about clock cycles measured in GHz.
- ☹ Because...

... computer architecture is real fun!



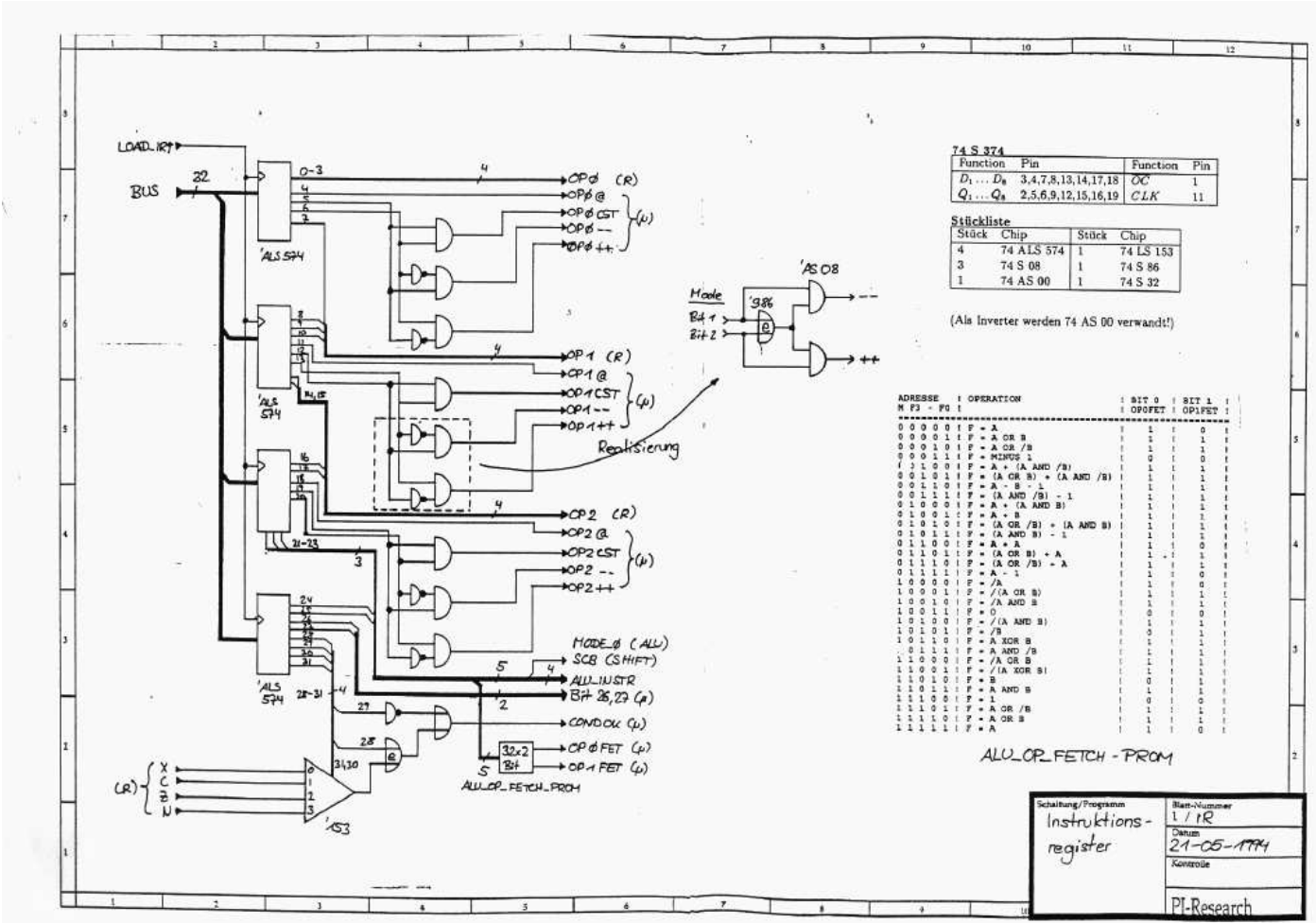
Requirements

- ☹ A simple, yet capable CPU architecture with no (or a few at maximum) idiosyncrasies in its instruction set, addressing modes, etc.
 - ⇒ I.e. *no* x86-CPU's suitable for that task.
- ☹ Use a processor not burdened by its history and the curse of compatibility.
 - ⇒ Develop a new processor, NICE, aimed for teaching the basics of computer architecture, the implementation of a CPU and assembler programming.

The NICE processor

- ☺ *Nice Is Charmingly Elegant*
- ☺ 32 bit processor
- ☺ 16 general purpose registers
- ☺ Three address instructions
- ☺ Predicative instructions (like ARM)
- ☺ Very simple instruction set
- ☺ Eight quite powerful addressing modes

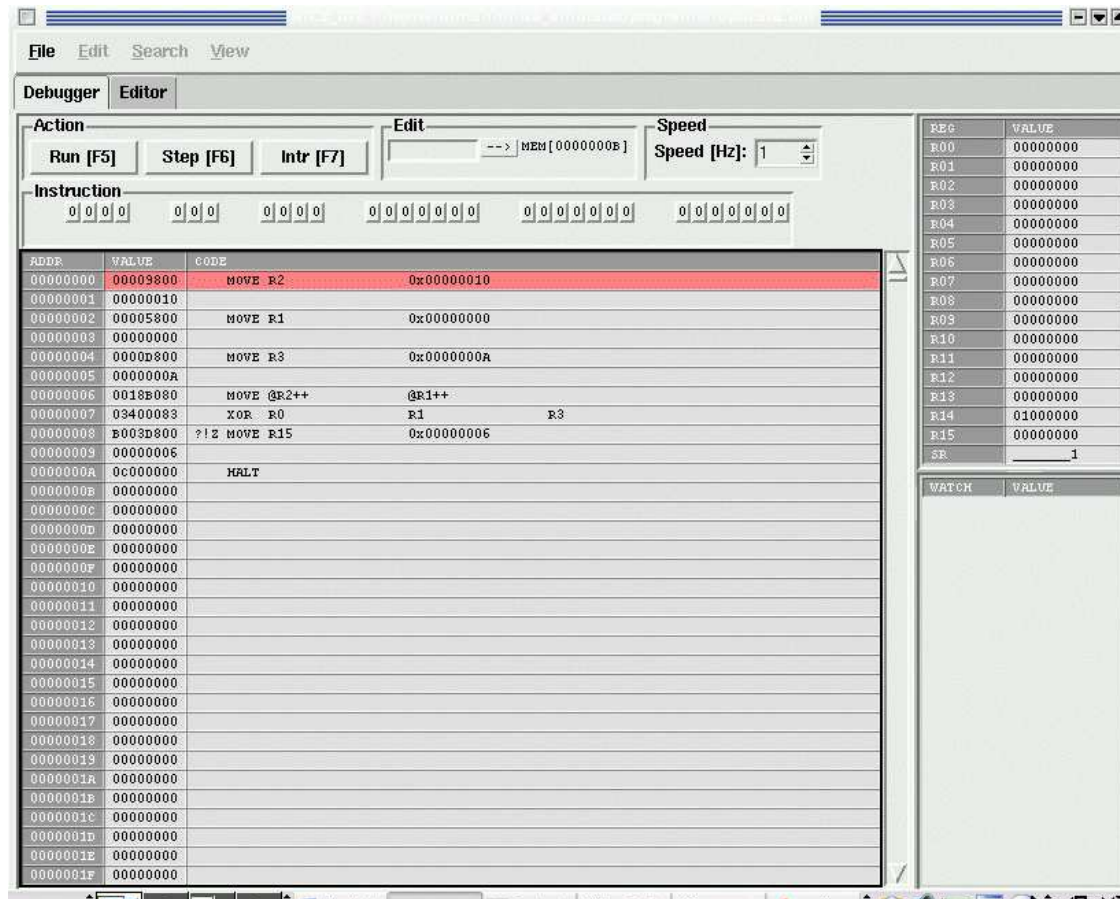
NICE – an impression



The emulator

- ☹ A hardware implementation was too bulky in the pre-FPGA era.
- ☹ A VAX-Fortran implementation of an emulator was not very user friendly – especially not when it comes to a hands-on-demonstration.
- ☹ In early 2004 I persuaded Thomas Kratz to write a new emulator in Perl together with me. (As it turned out, every line of code written by me became a victim of extensive code reviews and rewrites – so Thomas did the overwhelming part of programming: Thank you!)

The emulator – an impression



Resources

- ☞ <http://www.vaxman.de> (after this conference :-)).
- ☞ Bernd Ulmann, „NICE – an elegant and powerful 32-bit architecture“, in *Computer Architecture News*, OCT-1997.
- ☞ Bernd Ulmann, „Designing a NICE Processor“, in *Microprocessors and Microsystems*, Elsevier, Vol. 23, Oct. 1999, pp. 257-264.